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Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/801,234
Filing Date	March 16, 2004
First Named Inventor	Fu-Hsin CHEN
Art Unit	2826
Examiner Name	Dickey, Thomas L.
Attorney Docket Number	2003-0322 / 24061.79

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months. Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees

   The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☑ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 08-1394. I have enclosed a duplicate copy of this sheet.

      i. ☑ RCE fee required under 37 CFR 1.17(e)

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☐ Check in the amount of $ _____ enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	June 9, 2006
Name (Print/Type)	David M. O'Dell	Registration No.	42,044

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name (Print/Type)	Bonnie Boyle	Date	June 9, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	Attorney Docket No. 2003-0322 / 24061.79
Fu-Hsin Chen	§	
	§	Customer No. 42717
Serial No.: 10/801,234	§	
	§	Group Art Unit: 2826
Filed: March 16, 2004	§	
	§	Examiner: Dickey, Thomas L.
For: HIGH-VOLTAGE MOS TRANSISTOR	§	
AND METHOD FOR FABRICATING	§	Confirmation No.: 2028
THE SAME	§	

AMENDMENT FOR RCE

Mail Stop RCE
Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I. Introductory Comments

A Notice of Appeal was filed in the present application on March 28, 2006. By way of the attached request for RCE and the present amendment, the appeal for this application is withdrawn and further examination is requested in view of the following:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

II. Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-7. (Canceled)

8. (Original) A high-voltage MOS transistor comprising:

a substrate;

a gate structure overlying the substrate, the gate structure having a first side and a second side opposite to the first side;

a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure; and

a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region and a third doping region with the second dosage formed in the substrate adjacent to the edge of the second side of the gate structure to serve as a source region;

a channel region formed in the substrate between the first and third doping regions by turning on the high-voltage MOS transistor to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

9. (Original) The device as claimed in claim 8, wherein the gate structure is composed of a gate, a gate dielectric layer, and a gate spacer.

10. (Currently amended) ~~The device as claimed in claim 8,~~ A high-voltage MOS transistor comprising:

a substrate;

a gate structure overlying the substrate, the gate structure having a first side and a second side opposite to the first side;

a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure;

a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region and a third doping region with the second dosage formed in the substrate adjacent to the edge of the second side of the gate structure to serve as a source region; and

a channel region formed in the substrate between the first and third doping regions by turning on the high-voltage MOS transistor to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region,

wherein the first dosage is about 7.0 to 9.0E12 ions/cm^2.

11. (Original) The device as claimed in claim 10, wherein the second dosage is about 2.0 to 4.0E15 ions/cm^2.

12-23. (Cancelled)

24. (Currently amended) A high-voltage MOS transistor comprising:

a first drain region with a first dosage formed in a substrate, wherein the first drain region extends horizontally from a first point proximate to an upper surface of the substrate to a second point proximate to the upper surface;

a first source region with the first dosage formed in a substrate, wherein the first source region extends horizontally from a third point proximate to an upper surface of the substrate to a fourth point proximate to the upper surface;

a gate structure overlying the substrate, interposed between the first drain region and the first source region, ~~and~~ covering a portion of the first drain region extending from the first point to a fifth ~~third~~ point of the first drain region located between the first and second points, and covering a portion of the first source region extending from the third point to a sixth point of the first source region located between the third and fourth points;

a first spacer in contact with the gate structure and covering a portion of the first drain region from the fifth point to a seventh point of the first drain region located between the fifth and second points;

a second spacer in contact with the gate structure and covering a portion of the first source region from the sixth point to an eighth point of the first source region located between the sixth and fourth points;

a second drain region with a second dosage formed within the first drain region, wherein the second drain region extends substantially from the seventh ~~fourth~~ point to a ninth ~~fifth~~ point of the first drain region located between the seventh ~~fourth~~ and second points, and wherein the portion of the first drain region extending from the ninth ~~fifth~~ point to the second point is at substantially the same horizontal level in the substrate as the first point; and

a second source region with the second dosage formed within the first source region, wherein the second source region extends substantially from the eighth point to a tenth point of the first source region located between the eighth and fourth points, and wherein the portion of the first source region extending from the tenth point to the fourth point is at substantially the same horizontal level in the substrate as the third point, ~~a source region formed in a substrate on the opposite side of the gate structure from the first drain region,~~

~~———~~wherein a channel region formed in the substrate between the first drain region and the first source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region.

25. (Previously presented) The high-voltage MOS transistor of claim 24 further comprising a field oxide layer substantially abutting the first doped region at the second point.

26. (Currently amended) ~~The high-voltage MOS transistor of claim 24,~~ A high-voltage MOS transistor comprising:

a first drain region with a first dosage formed in a substrate, wherein the first drain region extends horizontally from a first point proximate to an upper surface of the substrate to a second point proximate to the upper surface;

a gate structure overlying the substrate and covering a portion of the first drain region extending from the first point to a third point of the first drain region located between the first and second points;

a spacer in contact with the gate structure and covering a portion of the first drain region from the third point to a fourth point of the first drain region located between the third and second points;

a second drain region with a second dosage formed within the first drain region, wherein the second drain region extends substantially from the fourth point to a fifth point of the first drain region located between the fourth and second points, and wherein the portion of the first drain region extending from the fifth point to the second point is at substantially the same horizontal level in the substrate as the first point; and

a source region formed in a substrate on the opposite side of the gate structure from the first drain region, wherein a channel region formed in the substrate between the first drain region and source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region,

wherein the first drain region has a doping concentration of approximately 7.0 to 9.0E12 ions/cm^2.

27. (Currently amended) ~~The high-voltage MOS transistor of claim 24,~~ A high-voltage MOS transistor comprising:

a first drain region with a first dosage formed in a substrate, wherein the first drain region extends horizontally from a first point proximate to an upper surface of the substrate to a second point proximate to the upper surface;

a gate structure overlying the substrate and covering a portion of the first drain region extending from the first point to a third point of the first drain region located between the first and second points;

a spacer in contact with the gate structure and covering a portion of the first drain region from the third point to a fourth point of the first drain region located between the third and second points;

a second drain region with a second dosage formed within the first drain region, wherein the second drain region extends substantially from the fourth point to a fifth point of the first drain region located between the fourth and second points, and wherein the portion of the first drain region extending from the fifth point to the second point is at substantially the same horizontal level in the substrate as the first point; and

a source region formed in a substrate on the opposite side of the gate structure from the first drain region, wherein a channel region formed in the substrate between the first drain region and source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region,

wherein the second drain region has a doping concentration of approximately 2.0 to 4.0E15 ions/cm^2.

28. (Currently amended) A high-voltage MOS transistor comprising:

a first drain region and a first source region formed in a substrate and spaced from each other;

a gate structure overlying the substrate, interposing between the first drain region and the first source region, and covering a first portion of the first drain region and a first portion of the first source region;

a first spacer in contact with the gate structure and covering a second portion of the first drain region adjacent to the first portion of the first drain region;

a second spacer in contact with the gate structure and covering a second portion of the first source region adjacent to the first portion of the first source region;

a second drain region formed within the first drain region, wherein the second drain region extends substantially from the second portion of the first drain region in the direction opposite the gate structure and the first spacer, wherein the portion of the first drain region extending beyond the second drain region is at substantially the same horizontal level in the substrate as the first portion of the first drain region; and

a second source region formed within the first drain region, wherein the second source region extends substantially from the second portion of the first source region in the direction opposite the gate structure and the second spacer, wherein the portion of the first source region extending beyond the second source region is at substantially the same horizontal level in the substrate as the first portion of the first source region, ~~a source region formed in a substrate on the opposite side of the gate structure from the first drain region,~~ wherein a channel region formed in the substrate between the first drain region and the first source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region.

29. (New) A high-voltage MOS transistor comprising:

a substrate;

a gate structure overlying the substrate, the gate structure having a first side and a second side opposite to the first side;

a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure; ~~and~~

a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region, the second doping region is offset from the first doping region at least by a first gate spacer;

~~and~~ a third doping region with the first dosage formed in the substrate on the second side of the gate structure and partially covered by the gate structure;

a fourth ~~third~~ doping region with the second dosage formed within the third doping region ~~in the substrate~~ adjacent to the edge on ~~of~~ the second side of the gate structure to serve as a source region, the fourth doping region is offset from the third doping region at least by a second gate spacer; and

a channel region formed in the substrate between the first and third doping regions by turning on the high-voltage MOS transistor to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

III. Remarks:

Claims 8-11 and 24-28 are pending. Claims 10, 24, 26, 27, and 28 have been amended. Claim 29 has been added. Claims 8, 9, 11, and 25 remain in their previous form.

Allowable Subject Matter

Noted with appreciation is the indication that Claims 10, 11, 26, and 27 recite allowable subject matter, and would be allowed if rewritten in independent form. Claims 10, 26, and 27 have been rewritten in independent form and Claim 11 remains in the original form since it depends on the Claim 10 which is now allowable.

Independent Claim 8

Independent Claim 8 stands rejected under 35 U.S.C. §102 as being anticipated by Hoshino et al. U.S. Patent No. 6,121,077. This ground of rejection is respectfully traversed. The PTO specifies in MPEP §2131 that, to anticipate a claim, a reference must teach each and every element recited in the claim. Claim 8 includes a recitation of:

> ... a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure; and
>
> a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region ...

It is respectively submitted that the Hoshino patent fails to disclose this precise structure. The Office Action asserts at lines 19-20 on page 2 that Figure 14a of Hoshino discloses

> a drain region (a second doping region 9 with a second dosage formed within the first doping region 8) adjacent to the edge on the first side of the gate structure;...

Applicant respectfully traverse this assertion since Hoshino clearly states in the specification on paragraph 211:

> a photoresist pattern (mask) PR4 is formed so as to cover a portion of the drain offset region 8 and the P type punch-through layer 3. Successively, impurities are introduced for forming the source.drain region by using the mask PR4.

The photoresist pattern PR4 is not part of the gate structure to a person skilled in the art. During a telephone interview, the examiner suggested that the photoresist pattern PR4 did the same "function" as a gate spacer, as used in the patent. Applicant's hereby assert that we are talking about structure, not a method. The examiner has not presented any evidence to support the allegation that photoresist is part of a "gate structure" in a "high-voltage MOS transistor". Therefore, the drain region is offset from the gate structure by the photoresist pattern (mask) PR4 and cannot be "adjacent to the edge on the first side of the gate structure". Hoshino thus does not disclose each and every element recited in Claim 8, and therefore does not anticipate Claim 8 under §102. Claim 8 is thus believed to be allowable over Hoshino, and notice to that effect is respectfully requested.

Independent Claims 24, 28 and 29

Independent Claims 24, 28 and 29 stand rejected under 35 U.S.C. §102 as being anticipated by Hoshino et al. U.S. Patent No. 6,121,077. Claims 24, 28 and 29 have been amended to describe a symmetric structure illustrated in Fig. 3e that the Hoshino reference does not teach.

Dependent Claims

Claims 9 and 25 respectively depend from Claim 8 and Claim 24, and are also believed to be distinct from the art of record, for example for the same reasons discussed above with respect to

Claims 8 and 24, respectively.

Conclusion

Based on the foregoing, it is respectfully submitted that all of the pending claims are fully allowable, and favorable reconsideration of this application is therefore respectfully requested.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

David M. O'Dell
Reg. No. 42,044

Dated: June 9, 2006

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R-132082.1

Certificate of Service

I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on June 9, 2006.

Bonnie Boyle